Dr. M Mohammed Sabir Hussain, PhD.

sabirhussain@mjcollege.com
+91 9849217818

In Brief:

- ✓ Working as Associate Professor and Associate head in the department of ECE

- ✓ 32 Research Publications (19 Conferences and 13 Journals) in which 6 journal are peer reviewed (Scopus Indexed and UGC approved journals) and few IEEE conference papers. Published one book on Low Power VLSI Design and Testing. Delivered 4 invited lectures in faculty development programs, in which 2 AICTE funded FDPs. Editorial Board Member and Reviewer for Journal of Communication Engineering and its Innovations AND Journal of Analog and Digital Communications, Reviewed research paper of the Journal of Engineering Research (TJER- SQU). Committee member and reviewer for International Conferences, Conducted faculty development programs (FDPs). Delivered technical talks as resource person in workshops and published one patent in the area of AI/ML.

- Orchid Id: https://orcid.org/0000-0002-8981-1584 (Documnets:4 Citations:8 H-Index:3)
- Scopus Id: https://www.scopus.com/authid/detail.uri?authorId=57210529236
- Google Scholar: https://scholar.google.com/citations?user=1h5vFAkAAAAJ&hl=en&authuser=1 (Documnets:24 Citations:19 H-Index:3 I10index:1)
- Research gate: https://www.researchgate.net/profile/Sabir-Hussain-17 (RG Score : 2.97)
- Puplons Id: https://publons.com/researcher/4217337/dr-m-mohammed-sabir-hussain/
- Scopus Author ID: 57210529236

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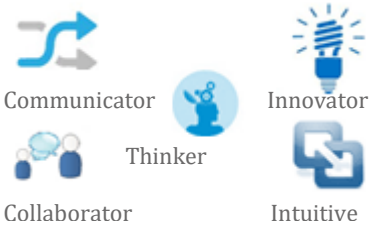
Key Skills

- Teaching & Mentoring
- Training & Development
- Curriculum Development
- Educational Assessment
- Research Work
- Classroom Presentations
- Students Management
- Relationship Management
- General Administration
- Team Management

Profile Summary

- **Ph.D., M.Tech. & B.Tech.** offering over **20 years** of pioneering experience and year-on-year success in achieving student's growth objectives in teaching & mentoring, research and administrative functions
- Expertise in implementing & delivering an appropriately broad, balanced, relevant & differentiated curriculum for students to support the teaching
- Actively engaged in **supervising & managing operational planning**& development, and directing day-to-day academic & associated operations
- **Exercises judgment** within generally defined practices in selecting methods & techniques for obtaining solutions through research
- **Dedicated leader** with proficiency in managing the administrative activities entailing event management, research works, exams, projects, workshops & conference; provided leadership on **35 UG Level and 10 PG Level Academics Projects**
- **Leader with merit of research article** getting published in peer reviewed journals and presenting papers in national and international conferences; *please refer annexure for detail*

Soft Skills



CareerTimeline

Shadan College of Engineering and Technology

Muffakham Jah College of Engineering

Education

- **Ph.D. (Electronics and Communication Engineering)** from Gandhi Institute of Technology And Management (GITAM) University Visakhapatnam, India in November 2019
- **M.Tech. (VLSI System Design)** from JNTU Hyderabad India in 2010 with 8/10 CGPA
- **B.Tech. (Electronics and Communication Engineering- ECE)** from JNTU Hyderabad India in 2004 with 7.2/10 CGPA

Recognitions

- Awarded Best Paper in the session Emerging Devices and Circuits-I for the paper entitled Memory Compiler Performance Prediction using RNN in IEEE 5th International conference on DevIC 2023.
- The Board of International Journal of Recent and Innovation Trends in Computing and Communication for the best paper presentation
- Excellence in Teaching and Learning awarded by Mission 10X in collaboration with Wipro Technologies, Hyderabad
- Certificate of Excellence in Research Paper Reviewing from Asian journals of advances in research certificate no: MBIMPH/PR/Cert/1099/MMS

Work Experience

December '2020 to till date with ECED, Muffakham Jah College of Engineering, Osmania University, Hyderabad, India as Associate Professor (4 Years)

August '2006 to Nov' 2020 till date with ECED, Muffakham Jah College of Engineering, Osmania University, Hyderabad, India as Associate Professor (14 Years)

Jun'2004 – Aug '2006 with ECED, Shadan College of Engineering and Technology, JNTU Hyderabad , India as Assistant Professor (2 years)

Key Result Areas:

- Providing leadership to teaching and administrative staff, ensuring high quality of teaching for postgraduate (PG) and undergraduate (UG) engineering students covering:
  - Digital Electronics (DE)
  - Digital System Design
  - Basic Electronics (BE)
  - Signal and System (SS)
  - Introduction to IoT(Arduino)
  - VLSI System Design
  - Electronic Workshop and Basic Circuit(PCB)
  - Electronic Device and Circuits
  - Verilog Hardware Description Language (FPGA)
  - Artificial Neural Networks/Machine Learning
  - Digital Signal Processing (DSP)
  - Fault Tolerant and Reliable Systems
- Spearheading curriculum planning, professional development and the implementation of educational programs
- Planning meetings, assisting teams with securing supplies and managing inter-departmental communications
- Reviewing the preset educational goals, objectives, classroom instructional programs, established academic and other performance objectives
- Developing educational standards & goals and educational quality management systems; establishing policies and procedures for smooth implementation
- Responding to the queries in a spontaneous manner, also counselling students and grooming them to attain their goals
- Evaluating curriculum, teaching methods & programs to determine their effectiveness and efficiency
- Instructing the students as per curriculum, thereby recognizing, respecting & nurturing their creative potential
- Interacting and collaborating with students, parents, and the community to build an environment that maximizes student learning, academic performance, and social growth
- Framing training objectives based on training needs after assessment of gap between skills already available & desired; conducting theoretical training programmes to enhance knowledge & skills
- Fostering success of all students by facilitating development, communication, implementation and evaluation of shared vision of learning that reflects excellence

Areas of Research Interest:

- 1. VLSI Testing; test pattern generations, data compressions with optimum DFT/BIST solutions using Test Compress 2. Development of programs on commonly available computing platforms and Advanced Tools like Tessent and Fastscan for DFT solutions to model multi-level faults at SOC level. 3. Fault Tolerant & Fault Testable Hardware Design: analysis, designs 4. Cryptosystems 5. Biomedical Applications, Bio-inspired Algorithms and Design of LFSRS 6. Secure scan design using FFSR 7. AI / ML for VLSI Design 8. FPGA based digital system design using Verilog-HDL 9. Low power IoT design and testing

Highlights:

- Provided guidance on following projects to Postgraduate Students
  - Neural Network Approach for Diagnosing the faulty functioning of digital circuits 2021
  - AI/ML/DL methods to predict power performance and area analysis in VLSI Circuits, 2021
  - Design of FFSR using Reversible Logic for secure scan design, 2020
  - Classification traffic signal signs using Deep Learning , 2020
  - An Efficient Low Power Delay Testing for Scan based BIST using SIC and X-Filling Techniques, 2018
  - Housing Price Prediction using Machine Learning, 2020.

- Design of low power and high fault Coverage TPG for scan BIST, 2017
- Low-Cost and High Power Reduction Approaches for Power Droop During Launch-On-Shift Scan-Based Logic BIS 2016
- A SIC Bit-Flipping Linear Feedback Shift Register for Low Power Built In Self-Test (BIST), 2015
- A Finite State Machine based LFSR for Low Power Built-In Self-Test (BIST)- 2014
- Design and Analysis of bit swapping LFSR for logical BIST built in self-2011-2012
- Efficient Built-in self-repair strategy for embedded SRAM, 2012-1013
- An efficient low power and high fault coverage FFSR using scan based-BIST, 2018

- Provided guidance on following projects to UG Students in Electronics and Communication Engineering
  - Predicting Momory Compiler Performance output using Recurrent Neural Networks, 2020
  - Design of Bit Swapping Linear Feedback Shift Register using Stacking technique for Low Power Application ,2019
  - Design of Feed Forward Shift (FFSR) Registers for Secure and Testable Scan, 2017
  - Multi clocked Linear Feedback Shift Registers for BIST, 2017
  - BISR Controller using BIST and BIAA, 2017
  - FSM Based LT-LFSR for Logic BIST, 2016
  - Deterministic built in self-test using linear feedback shift register, 2011-2012
  - FSM based Low Power Programmable Logic Built in Self-Test, 2012-2013
  - Design of bipartite LFSR for logic built in self-test controller, 2013-2014
  - Design and analysis of fault tolerant logic using triple modular redundancy, 2013-2014
  - Design of different Linear Feedback Shift Registers, 2014-2015
  - Design of different combinational benchmark circuits and testing, 2014-2015.
  - Design of low power BIST controller, 2014-2015

Thesis

- Ph.D. in the area of Low Power VLSI Design and Testing and the title of thesis is "Low Power SIC-X Filling TPG for Multi-model Fault Coverage using Scan Based BIST"; examined by:
  - Prof. Li Wen Zheng, Professor, Beijing University of Technology, China
  - Prof. Gaurav Trevidi Professor, Indian Institute of Technology (IIT) Guwahati, India
  - Prof. S. Varadharajan, Professor, SV University, India

Other Interest

- Delivered talks on:
  - A FDP programme on Digital System Design using Verilog HDL, conducted at MJ College of Engineering and Technology, Hyderabad, on 3rd and 4th June 2016, Telangana, India.
  - Introduction to Digital System Design using Verilog HDL and Demonstration using EDA tool, A FDP programme conducted at MJ college of Engineering and Technology, Hyderabad, on 5th July 2019, Telangana, India
  - A Resource person in 2 Week FDP on Research Methodology and Statistical Data Analysis Phase I Topic on Data Analysis using Python conducted by CBIT Hyderabad India on Feb 2020
  - A Resource person in 2 Week FDP on Research Methodology and Statistical Data Analysis Phase II ,Topic on Neural Networks Concept and Models conducted by CBIT Hyderabad India on Nov 2020.

IT Skills

- **Programming Languages:** Verilog HDL, System verilog HDL, PYTHON, Embedded C and C++
- **Packages:** MENTOR GRAPHICS, PSPICE, MATLAB, CADENCE EDA TOOL,TANNAR TOOL, MULTISIM, Tina Pro and XILINX ISE , FPGA and Advanced ARM Processors
- **Operating Systems:** Windows 9X/NT/ME/2000/XP, MS-DOS and Linux Red Hat 6

Professional Affiliations

- Life membership of Indian Society for Technical Education (ISTE) New Delhi registered code LM 68301
- Member of International Association of Engineers (IAENG) membership number is: 157280
- Editorial Board Member for:
  - Journal of Communication Engineering and its Innovations
  - Journal of Analog and Digital Communications
  - The Journal of Research and Engineering (TJER-SUQ) – Research Paper Reviewed
- As review committee member in International Conference on Recent Trends in Automation, 2018
- National advisory committee in International Conference on Recent. Advancement in Computer Science and Communication Technology. (ICRCSCT-18)
- Committee Member for International Conference On Applied Sciences, Engineering, Technology And Management

(ICASETM-18)

- Programme committee and review committee member for National Web Conference on Trends, Technological Challenges and Innovations in Engineering (TTCIE-2021)

Professional Associations

- Orchid Id: https://orcid.org/0000-0002-8981-1584 (Documnets:4 Citations:8 H-Index:3)
- Scopus Id: https://www.scopus.com/authid/detail.uri?authorId=57210529236
- Google Scholar: https://scholar.google.com/citations?user=1h5vFAkAAAAJ&hl=en&authuser=1 (Documnets:24 Citations:19 H-Index:3 I10index:1)
- Research gate: https://www.researchgate.net/profile/Sabir-Hussain-17 (RG Score : 2.97)
- Puplons Id: https://publons.com/researcher/4217337/dr-m-mohammed-sabir-hussain/

Personal Details

Date of Birth: 10th May 1982
Languages Known: English, Urdu and Telugu
Sex: Male
Marital status: Married
Number of dependent : Four (wife and 3 children)
Nationality: Indian
Passport Number: V1623392
Date of Expiry: 22/07/2031

Reference Details:

Prof. Afaq Ahmed

Department of Computers and Electrical Engineering , Sultan Qaboos University ,Oman

Email ID: afaq@squ.edu.om Cell: +968 99431341

Prof V Malleswara Rao
Professor, Department of ECE, GITAM University,
Visakhapatnam, Andhra Pradesh. India. Email: malleswararao.veera@gitam.edu

Dr.Mohammed Ismail

Department of Information Technology , Kannur University, Kerala, India

Email Id: mohammedismailb@kannuruniv.ac.in cell: +91 9440224793

Refer Annexure for Journal Papers & Conferences, Research Publications, Major Projects, Courses & Conferences

ANNEXURE

Journal Papers & Conferences

1. Mohammed Abdul Raheem, Mohammed Sabir Hussain, and Pathan Rehman Ahmed Khan, "ASIC Flow Implementation on a 32-bit RISC-V Processor using Cadence," *2024 IEEE EDKCON*, 30th Nov - 1st Dec 2024, Kolkata, India. (https://ieeexplore.ieee.org/document/10870604)
2. Mohammed Abdul Raheem, Kadiyam Sasidhar, and M. Sabir Hussain, "Smart Plant Monitoring System Using IoT," *Journal of Technology*, Vol. 12, Issue 6, 2024, pp. 928-932.
3. M. Sabir Hussain, M. Abdul Raheem, and M. Nasir Hussain, "A Novel Approach to Error Detection and Reliability in ALU Design using Word Voter TMR," *Proceedings of the 5th International Conference on Micro/Nanoelectronics Devices, Circuits & Systems (MNDCS-2025)*, NIT Silchar, India, Jan. 29-31, 2025. Published in *Springer Lecture Notes in Electrical Engineering (LNEE)*.
4. M. Sabir Hussain, M. Abdul Raheem, K. Sasidhar, and S. Ahmed, "FIFO Implementation in Manufacturing: Streamlining Production Processes and Minimizing Work-in-Progress Inventory," *Proceedings of the 1st International Conference on Microstructure, VLSI, Robotics, Communication, Electrical & Emerging Technologies using AI-ML Algorithms.*
5. **Dr.Sabir Hussain**, Dr. M.A Raheem and Prof. Afaq Ahmed published research article on topic " Machine Learning based Crop Recommendation on Cloud" in IEEE 8th I2CT Pune, India, the conference will be held on 07th-09th April 2023. (Scopus- Elsevier)

6. Dr. M.A Raheem, **Dr.Sabir Hussain** and Mr. Ayaan Ahmed published research article on topic "Memory Compiler Performance Using RNN" in IEEE DevIC 2023 Kolkata, India, the conference will be held on 08th-09th April 2023. (Scopus- Elsevier)

7. ***Sabir Hussain*** MA Raheem and Afaq Ahmed "SIC-TPG for path delay fault detection in BIST Application " presented and publish in IEEE International Conference "Devices for Integrated Circuits (DevIC 2021) on dated 19-20 May 2021 (Scopus- Elsevier)

8. Afaq ahmed , Sayyid samir al Busaidi,Mehdhat hussain ahmed awadallah, **Sabir Hussain** and Mazhar hussain " Designing of CRC Polynomials for 5G-NR" published and presented in 2nd International Hazar Scientific Researches Conference at Khazar University, Baku, Azerbaijan

9. Afaq ahmed , sayyid samir al busaidi,mehdhat hussain ahmed awadallah and S**abir Hussain** "FPGA – Chronological Developments and Challenges" published in international journal of electrical engineering & technology 12(11):60-72, november 2021.

10. ***Sabir Hussain*** and V Malleshwara Rao "An approach to Measure Transition Density of Binary Sequences For X-Filling based Test Pattern Generator in Scan based Design" published in "Journal of electrical and Computers engineering, issue. No 4, Vol.No. 8, Pg.No 2063-2071. (Scopus- Elsevier)
11. ***Sabir Hussain*** and V Malleshwara Rao "An Efficient SIC Generator using X Filling Techniques for Low Power Scan based BIST" publish in "Journal of simulation: Systems, Science & Technology, issue. No. 2., Vol.No 18, Pg.No 10.1-10.6 (Scopus- Elsevier)
12. ***Sabir Hussain*** and V Malleshwara Rao "A Path Delay Testing using SIC X-filling Technique for Multi Fault Modelling publishes in "International Journal of Pure and Applied Mathematics", issue. No 15, Vol.No 119, Pg.No 1543-1548. (Scopus- Elsevier)
13. ***Sabir Hussain*** and V Malleshwara Rao "A SIC-BS Linear Feedback Shift Register for Low Power BIST" Published in IEEE International Conference "Devices for Integrated Circuits (DevIC 2017) Indexed with (Scopus- Elsevier)
14. ***Sabir Hussain*** "Design of Low Power Multiplexer based LFSR for testing IoT Devices "Published in Journal of Information and Computational Science, Volume 9 Issue 10 – 2019. (Scopus- Elsevier)
15. ***Sabir Hussain*** "Design of Fault Tolerant ALU using word Voter Triple Modular Redundancy" accepted to published in Journal of Innovative Technology and Exploring Engineering, Volume-8 Issue-12(2019) (Scopus- Elsevier)
16. ***Sabir Hussain*** and PHST Murthy "A SIC Bit Flipping Linear Feedback Shift Register for Low Power BIST" published in "Journal of Instrumentation electrical electronics engineering (JIEEE-2015), Volume 3 Issue 3,e-ISSN: 2321-0621 p-ISSN: 2321-063X
17. ***Sabir Hussain*** and Syed Mohammed Ali Faraz "A New Multiplexer based LFSR for Low power BIST architecture"

presented in 3rd International conference on Innovations in electronics and communication engineering (ICIECE 2014), held during 18-19 July , 2014

18. ***Sabir Hussain*** and Padma Priya "Test Pattern Generator (TPG) for Low Power Logic Built In Self Test (BIST)", "Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering,Vol. 2, Issue 4, April 2013,pp.1634-1640 (Impact Factor 1.76)
19. ***Sabir Hussain*** and Kamal uz zaman "Design of Logic BIST using Bipartite LFSR", International Journal of Management, Information Technology and Engineering (BEST: JMITE) Vol. 1, Issue 3, Dec 2013, 79-84
20. ***Sabir Hussain***, Zakir Hussain & Kaleem Fatima "A VLSI Implementations of FSM-based programmable memory BIST Controller" International conference on Electronics and Communication Engineering April 28th -29th ,2012 Vizag ISBN 978-9381693-56-8.
21. ***Sabir Hussain***, Zakir Hussain & Kaleem Fatima "A VLSI Implementations of FSM-based programmable memory BIST Controller" accepted in IRNet Transaction on Electrical and Electronics Engineering (ITEEE- July 2012)
22. ***Sabir Hussain*** and Syed Mohammed Ali Faraz " Impact of the LFSR Seeding on Test Pattern Generator in BIST" accepted in Recent and Innovation Trends in Computing and Communication (JRITCC-2014).(Scientific Journal Impact Factor 5.098 and ISSN 2321-8169)
23. ***Sabir Hussain***, Afnan nisar, Afsha jabeen & Razia mohammadi "Design of Fault Tolerant ALU using Word Voter Triple Modular Redundancy" National Conference on Circuits, Signals and Systems (NCCSS) Jan 22th -24th 2015 Hyderabad ISBN 978-93-82570-47-9
24. ***Sabir Hussain***, Sk Zakeer and PHST Murthy "A SIC Bit Flipping Linear Feedback Shift Register for Low Power BIST" accepted in "International Conference on Recent Trends in Technology Research (2015)
25. Afsha Jabeen & ***Sabir Hussain*** "Design of Low power FSM based LFSR for Logic BIST, "Journal of Innovations in Engineering and Technology (JIET) ISSN 2919-1058, Nov 2016
26. Afsha Jabeen &***Sabir Hussain*** "Design of Low power FSM based LFSR for Logic BIST" First National Conference on Recent Trends in Engineering and Significance of Open Source Software (Special Issue NCRTEEFOOS 2016), December 15-17, 2016 , ISSN 2919-1058
27. ***Sabir Hussain*** and Dr V Malleshwara Rao "An Efficient Multiplexer based LFSR for Low Power DFT Architecture" presented in National conference on Advances in communication technologies (NCACT 2017)" organized by Department of Electronics and Communication Engineering GITAM University, Visakhapatnam, Andhra Pradesh, India during 24-25 March, 2017
28. ***Sabir Hussain*** and Dr V Malleshwara Rao " A path delay testing using SIC-X filling technique for multi fault modelling" presented in 8th International conference on Recent Engineering and Technology 2018, organized by Department of Electronics and Communication Engineering, OSIET, Chennai, India
29. ***Sabir Hussain*** and V Malleshwara Rao "A Review of Low Power and Area Efficient FSM based LFSR for Logic BIST" published in "Journal Electronic Design and Test" (JEDT 2017)
30. *MA Raheem* ***and Sabir Hussain*** "A Low voltage NMOS current bleeding down conversion mixer with source degeneration in 0.18 CMOS Technology " presented and publish in IEEE International Conference "Devices for Integrated Circuits (DevIC 2021) on dated 19-20 May 2021 (Scopus- Elsevier)
31. ***Sabir Hussain*** "Low power and High fault coverage SIC reseeding TPG using Xfilling scan based BIST", International Journal of Engineering and Technology Vol. 7, Issue 1.2, (2018), 220-224 (Scopus- Elsevier)
32. Afaq ahmed , Sayyid samir al Busaidi,Mehdhat hussain ahmed awadalla and **Sabir Hussain**" Design of A Gray Encoder using T-FFS and MUXS" published and presented in 2nd International Modern Scientific Research Congress at , Istanbul, Turkey, December 23-25, 2021.
33. Afaq Ahmad, Sabir Hussain, M A Raheem, Ahmed Al Maashri, Sayyid Samir Al Busaidi and Medhat Awadalla "ASIC vs FPGA based Implementations of Built-In Self-Test" Published in International Journal of Advanced Natural Sciences and Engineering Researches Volume 7, pp. 14-20, 6, 2023

Patent -1

- The patent Title: Prototype for detection and classification of pancreatic tumour using CNN feature based LLRBFNN Model published on 17/03/2023 (Patent Application No: 202341010490)

Book Publications -1

- Book Title: Low Power and High Fault Coverage Single Input Change X-Filling TPGs published by in LAMBERT Academic Publishing Germany (ISBN 978-620-0-29412-8)

Courses & Conferences

- Participated IN:
  - One-Week Online Faculty Development Program on Recent Trends in VLSI Conducted by Gokaraju Rangaraju Institute Of Engineering And Technology during 2-7 June 2020, Hyderabad.
  - One week FDP on "VLSI Fabrication Technology and IoT using Arduino" during 10th -16th March 2019 at University of Hyderabad.
  - Three days' workshop on "Set-up of IoT Lab during 25th to 27th March 2019 at MJCET, Hyderabad
  - One day Workshop on Overview of VLSI Front End Design and Verification held on 17th March 2018
  - Two Day workshop on Microwave Engineering" held on 3rd & 4th Jan 2018
  - One day workshop on "Internet of Things(IoT)" held on 28th November 2017 at MJCET, Hyderabad
  - International Conference on Devices for Integrated Circuit held on 23-24 March 2017
  - Three day OU Centenary International Conference Of ECE (Ou100ece) held on 28-30, December 2017
  - One Day "Workshop on Internet of Things" for faculties of MJCET held on 28th Nov. 2017
  - Half-day workshop on E Health Workshop conducted on 9th December 2016 by IEEE CAS Hyderabad Section.
  - "CAS PhD Forum" Organised by IEEE CAS/EDS Chapter, Hyderabad Section on 16th July 2016 at, Hyderabad, T.S.
  - One day workshop on "Digital Design through Arduino" organized by IIT Hyderabad Teaching Learning Centre and IEEE Hyderabad Section on 20th Feb 2016 at IIT Hyderabad.
  - 2 days International Conference ICMEET -2015 conducted by GITAM University, Vizag
  - Two week workshop on "Technical Communication" conducted by IIT Bombay
  - Two-day workshop on Research Design and Methodology on 14-15 March 2015 at GITAM Institute of Technology Vishakhapatnam, India
  - One day LATEX WORKSHOP conducted by MJCET held on August 2015
  - Two-day workshop on "Mathematical Technology" on 27th and 28th June 2018
  - Two-day workshop on "System on Chip (SoC) Design" held on 17th and 18th August 2013
  - Three day workshop on "Digital Signal Processing and Programming using MATLAB conducted by ECE dept JNTUH held on 27-29 January 2012.
  - Two-day ISTE workshop on "Aakash Tablet" Organized by IIT Bombay on 10th and 11th November 2012
  - Two days ISTE workshop on Writing Effective Conference Paper organized by IIT Bombay on 18th and 19th February 2012
  - One week ISTE workshop on Basic Electronics organized by IIT Bombay 28th June to 8th July 2011
  - One day workshop on Programmable System on Chip (PSoC3) held on 22nd December 2010
  - One day post workshop on In pursuit of excellence in engineering education through innovation conducted by Wipro Technologies Hyderabad held on November 19, 2009
  - Two day "National Conference on Intelligence System" organized by ECE department of Muffakham Jah College of Engineering and Technology Hyderabad held on 24-25 August 2007
  - Three-day workshop on teaching and learning methodologies and dale-Carnegie Training workshop on "high impact presentation skills" conducted by Wipro Technologies held on 26th to 30th November 2007
- Organized three day national level workshop on "Recent Trends In VLSI Design" held on 18th – 20th March 2010
- Presented a technical paper on "A New Multiplexer based LFSR for Low power BIST architecture" in 3rd International conference on Innovations in electronics and communication engineering (ICIECE 2014) in Gurunanak College on engineering and technology, Hyderabad
- Contributed as resource person and coordinator in two day workshop on "Digital System Design using Verilog" held on 4 and 5 June 2016
- Bagged Honour Code Certificate in "Technical Communication for Scientist" by IIT Bombay, an online course conducted held on 8 October to 18 November 2015
- Presented a technical paper on "A VLSI Implementations of FSM-based programmable memory BIST Controller" International conference on Electronics and Communication Engineering in Vizag, India