

**SCHEME OF INSTRUCTION & EXAMINATION  
B.E IV YEAR (REGULAR)**

**(INFORMATION TECHNOLOGY)**

**SEMESTER - I**

Sl. No.	Syllabus Ref.No	SUBJECT	Scheme of Instructions		Scheme of Examination		
			Periods per Week		Duration in Hrs	Maximum Marks	
			L/T	D/P		Univ. Exam	Sessi-onals
1.	BIT 401	<b>THEORY</b> VLSI Design	4	-	3	75	25
2.	BIT 402	Wireless & Mobile Communications	4	-	3	75	25
3.	BIT 403	Object Oriented System Development	4	-	3	75	25
4.	BIT 404	<b>ELECTIVE -II</b> Compiler Design	4	-	3	75	25
5.	BIT 405	Simulation & Modeling.					
6.	BIT 406	Client Server Programming					
7.	BIT 411	<b>ELECTIVE – III</b> Human Computer Interaction	4	-	3	75	25
8.	BIT 412	Intellectual Property Rights					
9.	BIT 413	Entrepreneurship					
1.	BIT 431	<b>PRACTICALS</b> Software Engg., Practicals	-	3	3	50	25
2.	BIT 432	VLSI Design Practicals	-	3	3	50	25
3.	BIT 433	Project Seminar	-	3	-	-	25
		<b>TOTAL</b>	<b>20</b>	<b>9</b>	<b>-</b>	<b>475</b>	<b>200</b>

**BIT-401**

**VLSI DESIGN**

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

**Unit –I**

An Overview of VLSI; logic design with MOSFETs, Physical structure of CMOS ICs; Fabrication of CMOS ICs.

**Unit –II**

Elements of Physical Design; Electrical Characteristics of MOSFETs; nFET current Voltage equations, the FETRC model , Modeling of small FETs; Electronic Analysis of CMOS logic gates; DC and switching characteristics of CMOS Inverter, Analysis of Complex logic gates, transmission gates and pass transistors.

**Unit –III**

Designing high-speed CMOS logic networks; Gate delays, Driving large capacitor loads, BI-CMOS drivers;

Advanced Techniques in CMOS logic circuits: Mirror circuits, Pseudo-nMOS, dynamic CMOS logic circuits;

System Specifications using Verilog HDL: Structural gate-level modeling, Behavioral and RTL modeling.

**Unit –IV**

General VLSI System Components: Multiplexers, Decoders, Encoder, Latches, Dlip-Flop, Registers, Role of Synthesis.

Arithmetic Circuits in CMOS VLSI: Adders, Multipliers.

Memories and Programmable logic: State and dynamic RAMs, ROM and logic arrays.

**Unit –V**

System –level Physical design: Interconnect delay modeling, Cross talk, Floor planning and routing, Power distribution and consumption, Design consideration.

VLSI Clocking and System Design: CMOS clocking styles, Pipelined systems, Clock generation and distribution.

Reliability and Testing of VLSI circuits: CMOS testing, test generation methods.

**Suggested Reading:**

1. John P. Uyemura, "Introduction to VLSI circuits and Systems", John Wiley & Sons, 2002.

**References:**

1. A. Puchnell, Douglas, "Basic VLSI Design" 3<sup>rd</sup> Edition, PHI.
2. Jan M. Rabey and others "Digital Integrated Circuits A design perspective ", Pearson Education, 2003.
3. R. L Geiger, P.E. Alleay etall, "VLSI Design techniques for Analog and Digital Circuits ", McGraw Hill, 1990.

**BIT-402**

**WIRELESS AND MOBILE COMMUNICATIONS**

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

**Unit –I**

Introduction to Wireless Communication Systems: Evolution of Mobile Radio Communications, Examples of Wireless Communication Systems.

Modern Wireless Communication Systems: Second Generation (2G) Cellular Networks, Third Generation (3G) Wireless Networks, Wireless local Loop, Wireless Local Area Networks.

The Cellular Concept: Introduction, Frequency Reuse, Channel Assignment Strategies, Handoff Strategies, Interference and Systems Capacity, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular Systems.

**Unit –II**

Mobile Radio Propagation : Large Scale - :Path Loss : Introduction to Radio Wave Propagation, Free Space Propagation Model, Three Basic Propagation Mechanisms, Reflection, Ground Reflection, Diffraction, Scattering, Outdoor Propagation Models, Indoor Propagation Models, Signal Penetration into Buildings.

**Unit –III**

Modulation Techniques for Mobile Radio: Digital Modulation, Linear Modulation Techniques, Constant Envelop Modulation, Spread Spectrum Modulation Techniques.

**Unit –IV**

Multiple Access Techniques for Wireless Communications: FDMA, TDMA, Spread Spectrum Multiple Access, Space Division Multiple Access, Capacity of Cellular Systems. Wireless Networking: Introduction, Difference between Wireless and Fixed Telephone Networks, Development of Wireless Networks.

Wireless Systems and Standards: Global System for Mobile (GSM), GPRS, CDMA Digital Cellular Standard.

### **Unit –V**

Mobile Network Layer: Mobile IP: Goals & Requirements, Terminology, Ip Packet Delivery, Agent Advertisement & Discovery, Registration, Tunneling and Encapsulation, Optimizations, Reverse Tunneling. Dynamic Host Configuration protocol.

Mobile Transport Layer: Traditional TCP, Snooping TCP, Mobile TCP, Fast Retransmit/Fast Recovery, Transmission/Time-Out Freezing, Selective retransmission, Transaction oriented TCP.

### **Suggested Reading:**

1. Theodore S. Rappaport, “Wireless Communications Principles and Practice “, 2<sup>nd</sup> Edition, Pearson Education, 2003.
2. Jochen Schiller, “Mobile communication”, Pearson Education Asia-2001.

### **BIT-403**

## **OBJECT ORIENTED SYSTEM DEVELOPMENT**

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

### **Unit –I**

Information systems: Problems in Information systems Development, Project life cycles, managing information system development, user involvement and methodological approaches, basic concepts and origins of object orientation modeling concepts.

### **Unit –II**

Requirement capture, requirement analysis, refining the requirement models, object interaction.

### **Unit –III**

Operations, control, design, system design.

### **Unit –IV**

Object design, design patterns, human computer interaction designing boundary classes.

### **Unit –V**

Data management design, implementation, reusable components, managing object oriented projects, system development methodologies.

**Suggested Reading:**

1. Simon Benett, Steve McRobb & Ray Farmer, "Object Oriented System Analysis and Design using UML", McGraw Hill, 2002.

**Reference:**

1. Frady Booch, James Rumbaugh, Ivor Jacobson, "The Unified Modeling Language-User guide", Addison Wesley 1999.
2. Ivor Jacobson, Grady Booch, James Rumbaugh, "The Unified software Development Process", Addison Wesley 1999.

**BIT-404**

**COMPILER DESIGN**

Instruction	4	Periods per week
Duration of University Examination	3	Hours
University Examination	75	Marks
Sessional	25	Marks

**Unit –I**

Deterministic Finite Automata and Non Deterministic Finite Automata, Finite Automata with e-moves, equivalence of Finite Automata and Regular Expressions.

Review of Grammars: Classification of grammars, Context free Grammars, Derivation trees, Simplification of Context Free Grammars, Left Recursion and Left Factoring.

**Unit –II**

Scanners : Scanning process, elementary scanner design . top down parsing. General top down parsing. Top down parsing with no back up. LL grammars. Error handling for top down parsing. Bottom up parsing. Polish expressions and their compilation,, operator precedence grammar.

**Unit –III**

LR Grammars. Error handling in LR Parsers. Comparison of parsing methods. Intermediate Code Generation : Intermediate language, Graphical Representation, Three Address code, Types of three addr. Statements, Syntax directed translation into three address code. Implementation of three addresses Statements.

**Unit –IV**

Assignment Statements: Names in the Symbol Table, Reusing Temporary names, Addressing Array elements, Type conversion with Assignments. Accessing fields in Records.

Boolean Expressions.

Run time environments: Source language issues, storage organization, storage-allocation strategies, and access to non-local names, parameter passing, symbol tables, language facilities for dynamic storage allocation, Dynamic storage Allocation Techniques.

### **Unit-V**

Code generation: Issues in the design of a code generator, The Target Machine, run – time storage management, Basic blocks and flow graphs, Next-use Information, A simple code generator, Register Allocation and Assignment.

The DAG Representation of basic blocks, peep hole optimization, Generating code for DAGs.

Code optimization: Introduction, principle sources of optimization, optimization of basic blocks, loops in flow graphs.

### **Suggested Reading:**

1. Alfred V. Aho, Ravi Sethi, Jeffrey D. Ullman, “Compilers: principals, techniques, and Tools “, Pearson Education, 2002.
2. Jean – Paul Trembly, Paul G. sorenson, “The Theory and practice of Compiler writing “, McGraw Hill, 1983.
3. John E. Hopcroft, Jeffery D. Ullman, “Introduction to Automata Theory, Languages and Computation”, Pearson education. 2002.

### **BIT-405**

### **SIMULATION AND MODELLNG**

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

### **Unit – I**

Systems and models, the concept of a system. System environment, Stochastic activities, Continuous and discrete systems, System modeling, types of models, static physical systems, dynamic physic models, static mathematical models, dynamic mathematical model, principles used in modeling.

### **Unit –II**

Continuous system simulation, a chemical reactor, simulation of a servo system, analog vs. digital simulation.

### **Unit-III**

Discrete system simulation, discrete events, representation of time, generation of arrival patterns, simulation of telephone system, delayed calls, simulation programming tasks.

#### **Unit-IV**

Random number generation, generation of uniformly distributed random numbers, the rejection method, tests for randomness.

#### **Unit –V**

Simulation languages, GPSS, Simscript II, Simula design and evaluation of simulation, experiments, length of simulation runs, verifications and validations of simulation.

#### **Suggested Readings:**

1. Deo N, "System simulation with digital Computer ", Prentice Hall, 1980.
2. Gordon G, "System Simulation", Prentice Hall, 1995.

Reference:

1. Averill M law and w. David Kelton, "Simulation Modeling and Analysis", McGraw Hill, Third Edn., 2000.

#### **BIT-406**

#### **CLIENT –SERVER PROGRAMMING**

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

#### **Unit-I**

Object –oriented programming with Java.  
Java fundamentals, Exceptions, Threads, Strings  
Making Applets Live on the Web  
Debugging Java Applets and Applications  
Windows and Menus  
Application Controls, Dialogs  
Fonts and Texts, Drawing Images and Image Processing, Animation  
Mouse Input

#### **Unit –II**

Stream I/O, Socket Interface  
RMI, RMI API  
Java Database Connectivity

### **Unit –III**

CORBA with Java  
Client/Server, CORBA-Style  
The Object Web: CORBA Meets Java

#### **I. The CORBA /Java ORBs**

ORBlets Meet Applets  
CORBA Initialization Protocol  
CORBA Activation Services  
Interface Repository  
CORBA IDL-to-Java

### **Unit –IV**

CGI, Servlets and RMI  
HTTP, 3-Tier CGI and State  
Life cycle of servlets, Servlets API

### **Unit –V**

Java Beans and EJB  
The Bean Component model  
Events, Properties, Persistency, Introspection of beans  
EJB frameworks, Session and entity beans,  
EJB/Container protocol,  
Support for transaction,  
EJB packaging, EJB design guide lines

#### **Suggested Reading:**

1. Orfli, Robert and Dan Harkey, “Client /Server Programming with Java and CORBA”, Second Edition, John Wiley & Sons, Inc., 1998.
2. Ivor Horton, “Beginning Java “, Wrox Publications.

### **BIT-411**

#### **HUMAN COMPUTER INTERACTION**

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

### **Unit –I**

Importance of the User interface. Characteristics of Graphical and Web User Interfaces.

User Interface Design Process – knowing the client, understanding business function, principles of good screen design.

## **Unit –II**

System menus and Navigation schemes. Kinds of windows, Device based controls, Screen based controls, Test and Messages.

## **Unit –III**

Feedback, guidance and Assistance, internationalization and Accessibility. Graphics, Icons and Images. Colors Layout windows and pages.

## **Unit –IV**

Interaction design- Introduction, goals, usability. Conceptualizing interaction – problem space, conceptual models, interface metaphors, interaction paradigms. Cognition, conceptual frameworks for cognition. Collaboration and communication Social mechanisms, conceptual frame works.

## **Unit –V**

Affective aspects, expressive interfaces, user frustration, agents. Process of interaction design- activities, characteristics, practical issues, life cycle models. Design, Prototyping and Construction – prototyping, conceptual design, physical design.

Evaluation – Introduction, frame work. Testing and Modeling users – kinds of tests, doing user testing, experiments, predictive models.

### **Suggested Reading:**

1. Wilbert O. Galitz – “The essential guide to user interface design”, Wiley Dreamtech, 2002.
2. Preece, Rogers, Sharp – “Interaction design”, John Wiley, 2002.

## **BIT-412**

### **INTELLECTUAL PROPERTY RIGHTS**

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

## **Unit –I**

Introduction: Meaning of Intellectual Property- Nature of I.P- Protection of I.P. Rights-kinds of Intellectual Property Rights –International Conventions of Intellectual Property Rights- patent

Treaty 1970, GATT 1994, TRIPS & TRIMS – International Organization for Protection of IPR – WTO, WIPRO, UNESCO.

**Unit –II**

Patents: Meaning of Patent- Commercial Significance – Obtaining of Patent – patentable Subject – matter – rights and obligations of Patentee – specification – Registration of patents – Compulsory licensing and licenses of rights – Revocation.

**Unit –III**

Industrial Designs: Definitions of Designs – Registration of Designs – Rights and Duties of Proprietor of Design – Piracy of Registered Designs.

**Unit –IV**

Trade Marks: Meaning of trademark – purpose of protecting trademarks Registered trade mark – procedure – passing off – Assignment and licensing of trade marks – Infringement of trademarks.

**Unit – V**

Nature, scope of copyright – Subject matter of copy right – Right conferred by copyright- Publication – Broad – casting, telecasting – computer programme – Database right – Assignment – Transmission of copyright – Infringement of copy right.

**Suggested Reading:**

1. Cornish W.R, “Intellectual Property Patents “, Copyright, Trademarks and Allied Rights, Sweet & Maxwell 1993.
2. P. Narayanan, “Intellectual Property Law “, Eastern law House 2<sup>nd</sup> Edn. 1997.
3. Robin Jacob & Daniel Alexander, “ A Guide Book to Intellectual Property Patents, Trademarks, Copy rights and designs, Sweet and Maxwell, 4<sup>th</sup> Edn.,1993.

**BIT – 413**

**ENTREPRENEURSHIP**

Instruction	4 Periods per week
Duration of University Examination	3 Hours
University Examination	75 Marks
Sessional	25 Marks

**Unit –I**

Indian Industrial Environmental – Competence, Opportunities and Challenge. Entrepreneurship and Economic growth. Small Scale Industry in India, Objectives, Linkage among small, medium and heavy industries, Types and forms of enterprises.

**Unit –II**

Identification and characteristics of entrepreneurs. Emergence of First generation entrepreneurs, environmental influence and women entrepreneurs. Conception and evaluation of ideas and their sources. Choice of Technology – Collaborative interaction for Technology development.

### **Unit –III**

Project formulation, Analysis of market demand, Financial and profitability analysis and technical analysis. Project financing in India.

### **Unit –IV**

Project Management during construction phase, project organization, project planning and control using CPM, PERT techniques. Human aspects of project management. Assessment of tax burden.

### **Unit –V**

Behavioral aspects of entrepreneurs : Personality – determinants, attributes and models. Leadership concept and models. Values and attitudes. Motivation aspects. Change behavior. Time Management : Various approaches of time management, their strengths and weakness. The urgency addition and time management matrix.

### **Suggested Reading:**

1. Vasant Desai, “Dynamics of Entrepreneurial Development and Management “, Himalayas Publishing House,1997.
2. Prasanna Chandra, “Project –Planning, Analysis Selection, Implementation and Review “, Tata McGraw Hill Publishing Co.Ltd, 1995.
3. Stephen R. Covey and Roger Merrill A., “First Things First”, Simon and Scheuster publication, 1994.
4. Sudha G.S, “Organizational Behaviour”, National Publishing House, 1996.

### **BIT-431**

#### **SOFTWARE ENGINEERING PRACTICLAS**

Instruction	3 Periods per week
Duration of University Examination	3 Hours
University Examination	50 Marks
Sessional	25 Marks

Select one of the Software System and develop the following using CASE Tools.

1. Use-Case diagram
2. Class diagrams
3. Sequence diagrams

4. Collaborative diagrams.
5. Software Requirement Specifications document (SRS)
6. Dynamic modeling and state diagram
7. Class specification with functions proto type specifications.
8. E-R diagram
9. Rest Data Generator
10. Component diagram
11. Software metrics and Cost estimation
12. Project planning using PERT/CPM.
13. Study of CVS, SCCS.

#### **BIT-432**

#### **VLSI DESIGN PRACTICALS**

Instruction	3 Periods per week
Duration of University Examination	3 Hours
University Examination	50 Marks
Sessional	25 Marks

Select one large information system / approach and device the following using CASE Tool.

1. Switch level modeling using Vetilog.
  - a). Logic Gates
  - b). AOI and OAI gates
  - c). Transmission gate
  - d). Complex logic gates using CMOS
2. Structural Gate-level modeling [with and Without delays] – Digital circuits using gate primitives – using Vexilog.
  - a). AOI gate
  - b). Half adder and full adders
  - c). MVX using tristate buffers
  - d). S-R latch etc.
3. Mixed gate –level and Switch-level modeling using Vexilog-usage of primitives, modules and instancing and understanding the hierarchical design.
  - a). Constructing a 4-input AND gate using CMOS 2-input NAND and Nor gates.
  - b). Constructing a decoder using CMOS 2-input AND gates and Not gates etc.
4. RTL Modeling of general VLSI system components.

- a). MUX using transmission gates and pass transistors
  - b). Decoders
  - c). Priority encodes
  - d). flip-flops            e). Registers
5. Synthesis of Digital Circuits [Understanding the concepts of applying the constraints such as area and adder
- a). Ripple carry adder and carry look-ahead adder
  - b). Register based multiplier and array multiplier
6. Modeling of MOSFET using SPICE [level 1 parameters] and Electronic circuit simulation using AIM- APICE and Micro-cap 7 (spectrum software).
7. Stick diagram and layout of masks using L-Edit or LASI editor.
8. Understanding the concepts of Design Rule checking and SPICE net list extraction suing L-edit /DRC tool.
9. CMOS clocking styles.
- a). Clock generation circuit            b). a dual Clock finite state machine
10. Fault Modeling for Stuck –at –0 and Stuck-at-1 faults and Test vector generation.